ABSTRACT

Intelligent admission control is achieved in a packet switch while minimizing the reduction in throughput. An array of limit values is stored in a memory of the switch and is accessed according to an indexing scheme. As each packet is received, an index is created and an associated limit value is retrieved for a one-step comparison with a corresponding status value read from a hardware register of the switch to determine whether or not to admit the packet. Accordingly, the number of conditional branches implemented in the microcode is greatly reduced and the packets are processed faster, which results in an increased throughput in the switch. An optional second comparison can be made based on a corresponding probability value stored in the array (with each limit value) before discarding a packet. A random number is compared to each probability value to determine whether to admit the associated packet.